ABSTRACT

In this invention a process for a flash memory cell and an architecture for using the flash memory cell is disclosed to provide a nonvolatile memory having a high storage density. Adjacent columns of cells share the same source and the source line connecting these sources runs vertically in the memory layout, connecting to the sources of adjacent columns memory cells. Bit lines connect to drains of cells in adjacent columns and are laid out vertically, alternating with source lines in an every other column scheme. Wordlines made of a second layer of polysilicon form control gates of the flash memory cells and are continuous over the full width of a memory partition. Programming is done in a vertical page using hot electrons to inject charge onto the floating gates. the cells are erased using Fowler-Nordheim tunneling of electrons from the floating gate to the control gate by way of inter polysilicon oxide formed on the walls of the floating gates.